IN THE CLAIMS:

Please amend the claims as follows:

1. (Currently Amended) An integrated module comprising:

a circuit;

a plurality of input/output terminals, each connected to a driver circuit for driving output signals and to a reception circuit for receiving input signals;

a first delay element with a first delay time, wherein the first delay element is capable of being one of:

(i) connected ~~into or disconnected from a~~ signal path of a circuit-internal signal~~, in order~~ to delay ~~or to accelerate~~ the circuit-internal signal~~, respectively~~; and

(ii) disconnected from the signal path to accelerate the circuit-internal signal;

a first test delay element at a first input/output terminal pair, wherein the first test delay element is constructed in a substantially similar manner to the first delay element; and

a test control unit configured to determine, in a test operation, ~~to determine~~ the first delay time by means of a signal ~~propagation time beween~~ propagation time between the two input/output terminals of the first input/output terminal pair.

2. (Currently Amended) The integrated module of claim 1, further comprising:

a second delay element with a second delay time different from the first delay time, wherein the first and second delay elements are separately capable of being a respective one of:

connected into ~~or disconnected from~~ the signal path of the circuit-internal signal ~~separately, in order~~ to delay ~~or to accelerate~~ the circuit-internal signal; and

disconnected from the signal path to accelerate the circuit-internal signal.

3. (Currently Amended) The integrated module of claim 2, further comprising:

a second test delay element at a second input/output terminal pair, wherein the second test delay element is constructed in a substantially similar manner to the second delay element; and

wherein the test control unit is further configured to, in [[a]] the test operation, determine the second delay time ~~by means of a signal propogation time beween~~ on the basis of the signal propagation time between the two input/output terminals of the second input/output terminal pair.

4. (Currently Amended) The integrated module of claim 3, further comprising:

a delay control unit coupled with the first and second delay elements ~~in order to~~ selectively delay [[or]] and accelerate the signal by selective connection [[or]] and disconnection of at least one of the first ~~and/or~~ and the second delay elements to the signal path; and

a non-volatile setting memory ~~in order~~ to store a setting value which determines the connection and the disconnection of the first and second delay elements by the delay control unit.

5. (Original) The integrated module of claim 3, wherein the two input/output terminals of the first and the second input/output terminal pair are arranged adjacent to one another.

6. (Currently Amended) The integrated module of claim 3, wherein the first test delay element and ~~and/or~~ the second test delay element ~~can be~~ are selectively switched on and off in accordance with the test control unit, ~~in order~~ to connect the first ~~and/or~~ and the second test delay element, selectively, to the respective input/output terminal pair only during the test operation.

7. (Currently Amended) The integrated module of claim 1, wherein the driver circuit and the reception circuit of each of the input/output terminals ~~can be~~ are selectively switched on/off in accordance with the test operation.

8. (Currently Amended) A method for setting a temporal position of a signal in a signal path of a circuit of an integrated module to a desired signal position, comprising:

in a test operation, measuring a first delay time of a first delay element in a signal path of an in-circuit signal by propagating ~~a singal~~ the signal through a first test delay element whose structure is substantially similar to the first delay element; and

selectively connecting [[or]] and disconnecting the first delay element to the signal path based on results of measuring the delay time of the first delay element.

9. (Currently Amended) The method of claim 8, further comprising:

in a test operation, measuring a second delay time of a second delay element in the signal path of the in-circuit signal by propagating ~~a singal~~ the signal through a second test delay element whose structure is substantially similar to the second delay element; and

selectively connecting [[or]] and disconnecting the second delay element to the signal path based on results of the measuring the delay time of the second delay element

10. (Currently Amended) The method of ~~claim 8~~ claim 9, wherein the respective switching-on/off of the first delay element and ~~and/or~~ the second delay element is carried out in such a way that [[the]] a total delay time due to the first and ~~and/or~~ the second delay element is set in accordance with the measured first delay time and the measured second delay time such that the signal position of the signal corresponds ~~as precisely as possible~~ to the desired signal position.

11. (Currently Amended) The method of claim 10, further comprising storing the setting determined with regard to the respective switching-on/off of the first delay element and ~~and/or~~ the second delay element in a non-volatile storage in the integrated module, allowing the temporal position of the signal to be retained.

12. (Currently Amended) The method of claim 11, wherein storing the setting determined with regard to the respective switching-on/off of the first delay element and ~~and/or~~ the second delay element in the non-volatile storage in the integrated module comprises modifying states ~~the state~~ of fuses.

13. (Original) The method of claim 8, wherein the test operation is performed during a manufacturing process.

14. (Currently Amended) A dynamic random access memory (DRAM) device, comprising:

one or more memory elements controlled by control signals having associated setup and hold times;

a plurality of input/output terminals, each connected to a driver circuit for driving output signals and to a reception circuit for receiving input signals;

a plurality of delay elements with corresponding delay times, each capable of being one of:

(i) connected into ~~or disconnected from~~ a signal path carrying one of the control signals~~, in order~~ to delay ~~or to accelerate~~ the one control signal~~, respectively~~; and

(ii) disconnected from the signal path carrying the one control signal to accelerate the one control signal;

a plurality of test delay elements, each arranged between input/output terminals and constructed in a substantially similar manner to one ~~of the delay elements~~ respective delay element; and

a test control unit configured to determine, in a test operation, ~~to determine~~ respective delay times of the delay elements ~~by means of a signal propagation times between~~ based on respective signal propagation times between the input/output terminals of the input/output terminal pairs.

15. (Currently Amended) The DRAM of claim 14, further comprising a delay control unit to selectively connect [[or]] and disconnect the delay elements to the signal path based on the delay times determined by the test control unit.

16. (Currently Amended) The DRAM of claim 15, further comprising a plurality of non-volatile storage elements to store settings indicating, to the delay control unit, which delay elements ~~should be~~ are connected [[or]] and disconnected, respectively, to the signal path.

17. (Original) The DRAM of claim 16, wherein the non-volatile storage elements are set during a manufacturing process.